2023

PHYSICS — HONOURS

Paper : CC-13

(Syllabus : 2019-2020)

[Digital Electronics]

Full Marks : 50

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer ***question no.*** **1** and ***any four*** questions from the rest.

1. Answer ***any five*** questions : 2×5

(a) What is monolithic IC?

(b) Convert the hexadecimal number C1.A to a binary number.

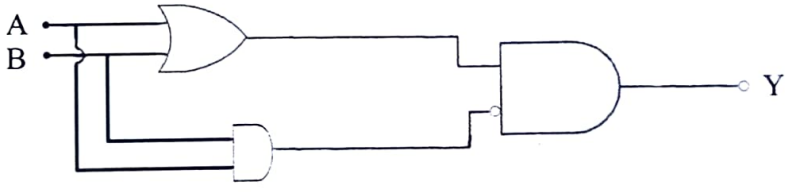
(c) Reduce the Boolean expression $Y = A\bar{B} + \overline{AB} + AB + \bar{A}\bar{B}$ in its simplest form.

(d) Which logic gate can be used as parity checker? Explain.

(e) Using 2's complement method subtract 00111 from 10101.

(f) Write at least two differences between latches and flip-flops.

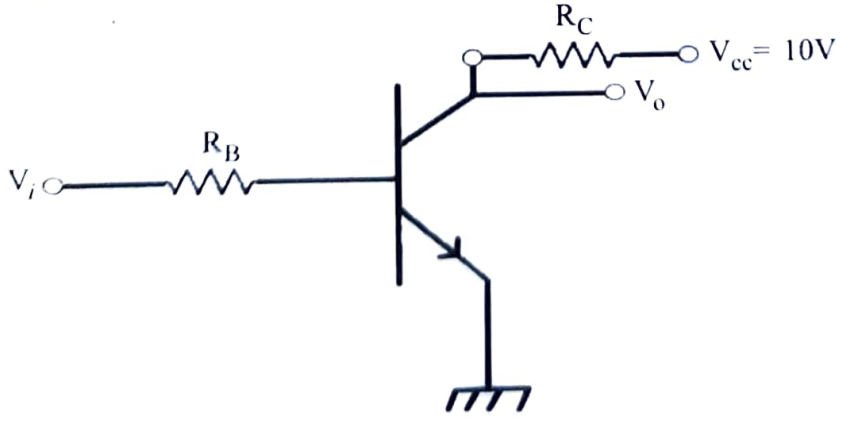
(g) Write the Boolean expression for the output Y in the following figure and simplify it.



2. (a) Draw the circuit diagram for realising AND gate using transistors.

(b) In the following NOT gate, calculate the base resistance (R_B) and collector resistance (R_C).

[Given : h_{FE} = 250, I_C(Sat) = 10 mA, V_{CC} = 10 V and V_i = 0 to 10V]



(c) Perform the binary operations : 11111 + 1011 – 111

Use 1's complement method for subtraction.

(d) What are the two advantages of higher density ICs? 2+3+3+2

3. (a) Simplify the following logic function in SOP form using K-map and implement it by using NAND gates only.

$$F(A, B, C, D) = \sum m(0, 2, 3, 5, 7, 8, 12, 13)$$

(b) Implement XOR gate using NOR gates only and give its truth table.

(c) Write two advantages of CMOS logic over TTL logic. (3+2)+(2+1)+2

4. (a) Show that a full adder circuit can be realised using half adders and an OR gate.

(b) What is a demultiplexer? Draw the block diagram of a 4 to 16 line demultiplexer.

(c) Using a 3 to 8 decoder and an OR gate, draw the circuit diagram to realise the following Boolean functions simultaneously : $F_1(A, B, C) = \sum m(0, 4, 6)$ and $F_2(A, B, C) = \sum m(1, 2, 3, 7)$.

3+(1+2)+4

5. (a) Draw the circuit diagram of a clocked SR-Flip-flop. How does the trigger pulse controls the change of state of this flip-flop? Explain.

(b) Discuss the differences between D and T type flip-flops using block diagrams and truth-tables.

(c) Convert an SR flip-flop into a JK flip-flop. [circuit diagram only] (2+2)+(2+2)+2

6. (a) Draw the block diagram of a 4-bit SISO shift register.

(b) The clock frequency is 2 MHz. How long will it take to serially load an 8-bit shift register?

(c) The bit sequence 0010 is serially entered (right most bit first) into a 4-bit parallel out left shift register that is initially clear. What are the outputs after two clock pulses?

(d) Draw the circuit diagram and explain how to convert a MOD-16 counter to a decade counter.

2+2+(1+1)+(2+2)

7. (a) What is A/D conversion? Find the output voltage from a 5-bit ladder that has a digital input of 11101.
[Take state 0 = 0V, State 1 = +10V.]

(b) Write at least two differences between RAM and ROM.

(c) Implement the following Boolean function using Programmable Logic Array (PLA).

$F = A + \bar{C}B$. (2+3)+2+3

$A\bar{C}\bar{D}$